WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:

forming an opening in a porous dielectric layer comprising a first low-k material overlying a substrate, the opening defined by sidewalls of the porous dielectric layer having exposed pores;

sealing exposed pores in the sidewalls by depositing:

a swelling agent lining the sidewalls and heating to swell the porous dielectric layer;

an adhesion promoter lining the sidewalls; or

a layer of dielectric material on the sidewalls; and

depositing a barrier metal layer lining the opening.

2. The method according to claim 1, further comprising:

filling the opening with metal; and

conducting chemical mechanical polishing (CMP) such that an upper surface of the metal filling the opening is substantially coplanar with an upper surface of the porous dielectric layer.

3. The method according to claim 2, comprising:

forming the opening as a dual damascene opening;

filling the opening with copper (Cu) or a Cu alloy as the metal, wherein the porous dielectric layer has a dielectric constant (k) less than 3.5.

4. The method according to claim 1, comprising depositing the swelling agent, adhesion promoter or layer of dielectric material at a thickness substantially equal to a largest dimension of the exposed pores.

5. The method according to claim 4, comprising depositing the swelling agent, adhesion promoter or layer of dielectric material at a thickness of 10Å to less than 300Å.

6. The method according to claim 5, comprising depositing the swelling agent, adhesion promoter or layer of dielectric material at a thickness of 10Å to 250Å.

7. The method according to claim 1, comprising sealing the pores by depositing an adhesion promoter lining the sidewalls.

8. The method according to claim 1, comprising sealing the pores by:

depositing a swelling agent lining the sidewalls;

heating to swell the porous dielectric layer; and

rinsing with water.

9. The method according to claim 8, comprising heating at a temperature of 25°C to 200°C.

10. The method according to claim 1, comprising sealing the pores by depositing a layer of dielectric material on the sidewalls.

11. The method according to claim 10, comprising depositing a layer of dielectric material which is the same as the first low-k material.

12. The method according to claim 11, wherein the first low-k material has a first porosity, the method comprising depositing a layer of dielectric material which has a porosity substantially the same as the first porosity.

13. The method according to claim 11, comprising depositing a layer of dielectric material which is substantially non-porous.

14. The method according to claim 10, comprising depositing a layer of dielectric material which is a material different from the first low-k material.

15. The method according to claim 14, wherein the first low-k material has a first porosity, the method comprising depositing the layer of dielectric material having a porosity substantially the same as the first porosity.

16. The method according to claim 14, comprising depositing a layer of dielectric material which is substantially non-porous.

17. A semiconductor device comprising:

a porous dielectric layer, comprising a first low-k dielectric material, overlying a substrate;

inlaid metal filling an opening in the porous dielectric layer, the opening defined by sidewalls of the porous dielectric layer with exposed pores, and

a layer of low-k dielectric material on the sidewalls with an interface therebetween, wherein the metal filling the opening comprises a barrier metal layer lining the opening and on the barrier metal liner filling.

18. The method according to claim 17, wherein the layer of low-k dielectric material comprises a dielectric material which is the same as the first low-k dielectric material and is either substantially non-porous or has a porosity substantially the same as that of the first material.

19. The method according to claim 17, wherein the layer of low-k dielectric material comprises a dielectric material which is different from the first low-k dielectric material and is either substantially non-porous or has a porosity substantially the same as that of the first low-k material.

20. The semiconductor device according to claim 17, wherein the layer of low-k dielectric material has a thickness of 10Å to less than 300Å.